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ABSTRACT OF THE DISCLOSURE

A gate electrode and a gate insulating film are formed for each of PMOSFET, NMOSFET and ferroelectric FET. Source/drain regions are defined for the NMOSFET and ferroelectric FET and for the PMOSFET by performing ion implantation processes twice separately. An intermediate electrode connected to the gate electrode of the ferroelectric FET, a ferroelectric film and a control gate electrode are formed over a first interlevel dielectric film. An interconnect layer, which includes first and second interconnects and is connected to the gate electrodes of the CMOS device, is formed on a second interlevel dielectric film. The first and second interconnects are connected to the control gate and intermediate electrodes of the ferroelectric FET, respectively.